800G QSFP-DD DR8 Pluggable Optical Transceiver

Features

- QSFP-DD800 MSA and CMIS 4.0 compliant
- MPO-16 APC connector
- 8x106.25Gbps (53.125GBd PAM4) electrical interface
- 8x106.25Gbps (53.125GBd PAM4) optical interface
- Up to 500m over SMF
- Power dissipation ≤ 16W
- Operating case temperature: 0°C to 70°C
- IEEE 802.3cu and IEEE 802.3ck compliant
- Built-in digital diagnostic functions
- 3.3V power supply voltage
- RoHS compliant

Applications

- 800G Ethernet
- Data center networks

Product Description

The Hyper Photonix HSD2-800-DR-P8S transceiver is designed for 800G Ethernet communication application links over 500m of single-mode fiber(SMF), and it is compliant with QSFP-DD800 MSA, 800G Pluggable MSA, CMIS 4.0, IEEE 802.3cu, and 802.3ck standards. The optical signal is transmitted over eight parallel channels at a central wavelength of 1310nm. The module contains 8 parallel channels on the transmitter and receiver, each operating at 106.25Gbps. It is suitable for 800G Ethernet, Data Center, Breakout 2x400G DR4 or 8x100G DR Application. The optical interface is MTP/MPO-16 APC connector.

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{cc}	-0.5	-	3.6	V
Storage Temperature	T_{sto}	-40		85	°C
Relative Humidity (Non-condensing)	RH	5		95	%
Control Input Voltage	V_i	-0.3		V_{cc}+0.5	

NOTE: Exceeding these ratings may damage the devise permanently.

Specified Operations Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V_{cc}	3.135	3.3	3.465	V
Case Operating Temperature	T_{op}	0	-	70	°C
Relative Humidity (Non-condensing)	RH	15		85	%
I2C Clock Frequency			100	400	kHz

Electrical Characteristics

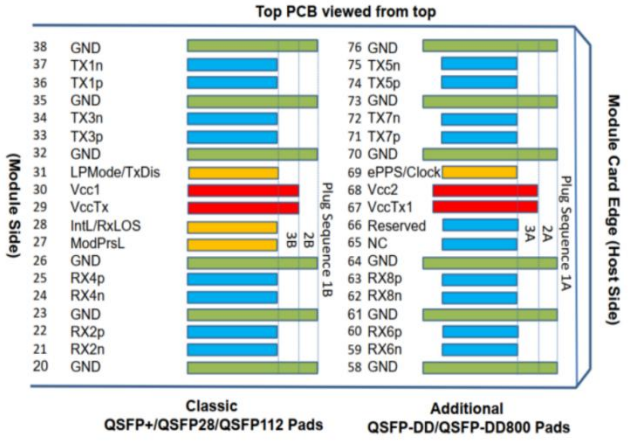
Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Current	I_{cc}			5118	mA
Power On Initialization Time	T_{init}			2000	ms
Transmitter					
Signaling Speed, each lane			53.125		GBd
Signaling Speed Tolerance		-100		+100	ppm
Differential pk-pk input voltage tolerance	$V_{in,pp}$	750			mV
AC common-mode RMS voltage tolerance		25			mV
Differential Input Impedance	Z_{in}	90	100	110	Ohms
Effective return loss	ERL	8.5			dB
Single-ended voltage tolerance range		-0.4		3.3	V
DC Common Mode Voltage		-0.35		2.85	V
Receiver					
Signaling Speed, each lane			53.125		GBd
Signaling Speed Tolerance		-100		+100	ppm
Differential pk-pk output voltage Short mode Long mode	$V_{out,pp}$			 600 845	mV
Eye Height	EH	15			mV
Differential Output Impedance	Z_{out}	90	100	110	Ohms
Transition Time, 20% to 80%	T_r, T_f	8.5			ps
DC Common Mode Voltage		-0.35		2.85	V
AC Common Mode output Voltage (RMS)		25			mV

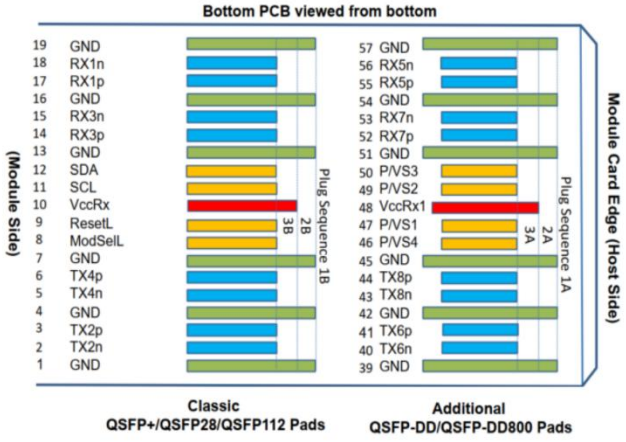
Optical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Transmitter						
Signaling Speed			53.125		GBd	1
Signaling Speed Tolerance		-100		+100	ppm	
Modulation Format			PAM4			
Wavelength	λ	1304.5	1311	1317.5	nm	
Side Mode Suppression Ratio	SMSR	30			dB	
Average TX Power	P_{avg}	-2.9		4	dBm	1
Outer Optical Modulation Amplitude	OMA_{outer}	-0.8		4.2	dBm	1
Extinction Ratio	ER	3.5			dB	1
Avg Launch Power TX Off	P_{off}			-15	dBm	1
Launch Power in OMA_{outer} – TDECQ for extinction ratio ≥5dB for extinction ratio <5dB		 -2.2 -1.9			 dBm dBm	1
Transmitter & Dispersion Eye Closure	TDECQ			3.4	dB	1
TDECQ-$10log_{10}(C_{eq})$				3.4	dB	
Relative Intensity Noise	RIN			-136	dB/Hz	
Optical Return Loss	ORTL			15.5	dB	
Reflectance				-26	dB	
Receiver						
Signaling Speed			53.125		GBd	1
Signaling Speed Tolerance		-100		+100	ppm	
Modulation Format			PAM4			
Wavelength	λ	1304.5	1311	1317.5	nm	
Damage Threshold		5			dBm	1
Average RX Power		-5.9		4	dBm	1
RX Power (OMA_{outer})				4.2	dBm	2
RX Reflectance				-26	dBm	
RX Sensitivity (OMA_{outer})				Max(-3.9, SECQ-5.3)	dBm	3,4
Stressed RX Sensitivity (OMA_{outer})				-1.9	dBm	1
Conditions of Stressed RX Sensitivity Test						
Stressed Eye Closure, lane under test	SECQ		3.4		dB	
OMA_{outer} of Each Agressor Lane			4.2			

1. *Each lane.*
2. *Receiver sensitivity (OMAouter) each lane (max) is informative and is defined for a transmitter with SECQ of 0.9 dB.*
3. *Measured with conformance test signal at TP3 for BER=2.4x10^{-4}.*
4. *Receiver sensitivity (OMAouter),each lane (max) is informative and is defined for a transmitter with a value of SECQ up to 3.4 dB.*

Electrical Input/Output





QSFP-DD800 Module contact pad electrical definition

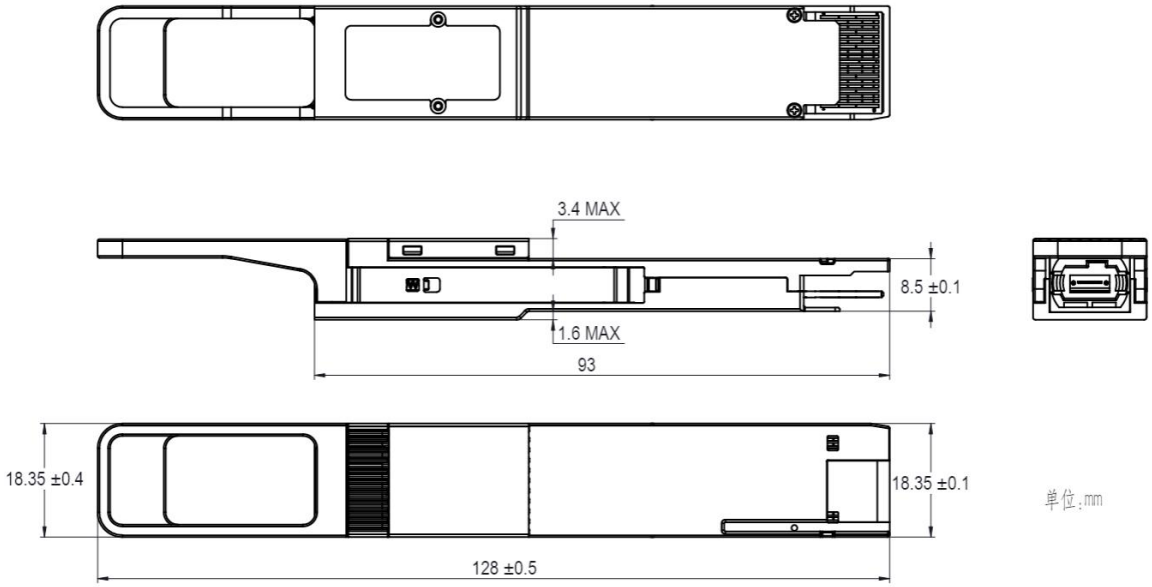
PIN	Logic	Symbol	Description	Notes
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	
7		GND	Ground	1
8	LVTTL-I	ModSelL	Module Select	
9	LVTTL-I	ResetL	Module Reset	
10		VccRx	+3.3V Power Supply Receiver	2
11	LVCOMS-I/O	SCL	2-wire serial interface clock	
12	LVCOMS-I/O	SDA	2-wire serial interface data	
13		GND	Ground	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Input	
15	CML-O	Rx3n	Receiver Inverted Data Input	
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Input	
18	CML-O	Rx1n	Receiver Inverted Data Input	
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Input	
22	CML-O	Rx2p	Receiver Non-Inverted Data Input	

23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Input	
25	CML-O	Rx4p	Receiver Non-Inverted Data Input	
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	
28	LVTTL-O	IntL/RxLOS	Interrupt/Optional RxLOS	
29		VccTx	+3.3V Power supply transmitter	2
30		Vcc1	+3.3V Power supply	2
31	LVTTL-I	LPMode/TX Dis	Low Power Mode/optional TX Disable	
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	
34	CML-I	Tx3n	Transmitter Inverted Data Input	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	
37	CML-I	Tx1n	Transmitter Inverted Data Input	
38		GND	Ground	1
39		GND	Ground	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	
42		GND	Ground	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	
45		GND	Ground	1
46	LVCOMS/CML-I	P/VS4	Programmable/Module Vendor Specific 4	4
47	LVCOMS/CML-I	P/VS1	Programmable/Module Vendor Specific 1	4
48		VccRx1	3.3V Power Supply	2
49	LVCOMS/CML-O	P/VS2	Programmable/Module Vendor Specific 2	4
50	LVCOMS/CML-O	P/VS3	Programmable/Module Vendor Specific 3	4
51		GND	Ground	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Input	
53	CML-O	Rx7n	Receiver Inverted Data Input	
54		GND	Ground	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Input	
56	CML-O	Rx5n	Receiver Inverted Data Input	
57		GND	Ground	1
58		GND	Ground	1
59	CML-O	Rx6n	Receiver Inverted Data Input	
60	CML-O	Rx6p	Receiver Non-Inverted Data Input	
61		GND	Ground	1
62	CML-O	Rx8n	Receiver Inverted Data Input	

63	CML-O	Rx8p	Receiver Non-Inverted Data Input	
64		GND	Ground	1
65		NC	No Connect	3
66		Reserved	For future use	3
67		VccTx1	3.3V Power Supply	2
68		Vcc2	3.3V Power Supply	2
69	LVCOMS-I	ePPS/Clock	1PPS PTP clock or reference clock input	5
70		GND	Ground	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	
72	CML-I	Tx7n	Transmitter Inverted Data Input	
73		GND	Ground	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	
75	CML-I	Tx5n	Transmitter Inverted Data Input	
76		GND	Ground	1

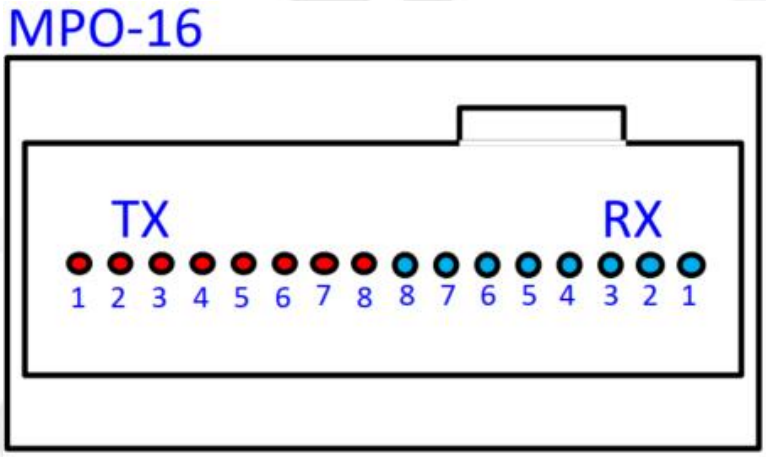
1. *QSFP-DD uses common ground (GND)for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.Each connector Gnd contact is rated for a steady state current of 500mA.*
2. *VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Supply requirements defined for the host side of the Host Card Edge Connector are listed in Table 13. For power classes 4 and above the module differential loading of input voltage pads must not result in exceeding contact current limits. Each connector Vcc contact is rated for a steady state current of 1500 mA.*
3. *Reserved pad recommended to be terminated with 10 k to ground on the host. Pad 65 (No Connect) Shall be left unconnected within the module, optionally pad 65 may get terminated with 10 k to ground on the host.*
4. *Full definitions of the P/VSx signals currently under development. For module designs using programmable/vendor specific inputs P/VS1 and P/VS4 signals it is recommended each to be terminated in the module with 10 k. For host designs using programmable/vendor specific outputs P/VS2 and P/VS3 signals it is recommended each to be terminated on the host with 10 k.*
5. *for host not implementing ePPS/Clock, it is not necessary to parallel terminate the ePPS/Clock signal to ground on the host. ePPS/Clock already has parallel termination in the module.*

Mechanical Specifications



Product shall be of design, construction, and physical dimensions specified on the applicable product drawing.

Optical Interface



Laser Safety

This is a Class 1 Laser Product as defined by IEC 60825-1:2014. When operated within the limits of this specification it is considered non-hazardous. Operating this product in a manner inconsistent with specifications and intended usage may result in hazardous radiation exposure.

Product Label

Regulatory Certifications

This product is certified to the following regulatory standards:

Category	Standard
Radiated Emissions	EMC Directive 2014/30/EU EN 55032 CISPR 32 FCC rules 47 CFR Part 15 ICES-003 VCCI-CISPR 32 AS/NZS CISPR 32
Radiated Immunity	EMC Directive 2014/30/EU EN 55035 CISPR 35 IEC/EN 61000-4-3
RoHS	EU RoHS (2011/65/EU & (EU) 2015/863) & UK RoHS EN IEC 63000:2018 & BS EN IEC 63000:2018
Flammability (PCB)	UL Class 94 V-0

Ordering Information

Part No.	Data Rate	Wavelength	Max Distance	Case Temperature Range
HSD2-800-DR-P8S	850Gbps	1310nm	500m	0°C to 70°C

Notice

Hyper Photonix reserves the right to change specifications of products identified in this datasheet without notice. Applications described herein are for illustrative purposes only, and Hyper Photonix makes no warranty that identified products will be suitable for the described applications without further testing and/or modification.

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Revision History

Version	Description of Change	Approvals	
		Name	Date
Preliminary Version	Preliminary Release	Henry Plaessmann	6/29/2023